AMENDMENTS TO THE CLAIMS

1. (Previously Presented) An integrated circuit (IC) having programmable interconnections, comprising:

a first plurality of regions, each region having a programmable circuit with a programmable function; and

a second plurality of areas of the IC, wherein each area of the second plurality extends from one edge of the IC to an opposing edge of the IC, and wherein each area of the second plurality comprises predetermined regions of the first plurality, wherein the predetermined regions in an area are in a column and substantially fill the area, and wherein each of the predetermined regions in a first area comprises programmable circuits which are substantially identical and have a first function and each of the predetermined regions in a second area comprises programmable circuits which are substantially identical and have a second function.

2. (Previously Presented) The integrated circuit of claim 1 further comprising a third area of said second plurality of areas wherein every predetermined region in the predetermined regions in the third area has a circuit of only one circuit type, the circuit type selected from a group consisting of Configurable Logic Block (CLBs), Multi-Giga Bit Transceivers (MGTs), Block Random Access Memories (BRAMs), Digital Signal Processor (DSP) circuits, Multipliers, and Input/Output Blocks (IOBs).

3. (Previously Presented) The integrated circuit of claim 1 wherein an area of the second plurality has predetermined regions comprising Multi-Giga Bit Transceiver (MGT) circuits.

4. (Previously Presented) The integrated circuit of claim 1 further comprising a heterogeneous area of said second plurality of areas of the IC, the heterogeneous area having regions with programmable circuits that are of different circuit types.

5. (Previously Presented) A die having an integrated circuit, comprising:

a first set of regions, each region in the first set having an Input/Output circuit;

a second set of regions, each region in the second set having a circuit with a programmable logic function;

a third set of columns, wherein a top of each column of the third set is positioned at a top side of the die and a bottom of each column of the third set is positioned at a bottom side of the die;

a first column of the third set, wherein each region of the first column consisting essentially of regions from the first set; and

a second column of the third set consisting essentially of regions from the second set, wherein the second column is interposed between the first column and a nearest side edge of the die.

6. (Previously Presented) The die of claim 5 wherein an Input/Output circuit comprises a Multi-Giga Bit Transceiver or an input/output block or a combination thereof.

7. (Previously Presented) The die of claim 5 further comprising a third column of the third set positioned at a center line of the die, the third column comprising assorted tiles.

Claims 8-20. (Cancelled)

21. (Currently Amended) A method, comprising:

providing a plurality of configurable logic blocks in a first column <u>having the same function</u>, the first column extending from a first side of an integrated circuit die to a second side of the integrated circuit die; [[and]]

providing a plurality of Input/Output blocks in a second column, the second column extending from the first side of the integrated circuit <u>die</u> to the second side of the integrated circuit <u>die; and</u>

<u>providing a plurality of tiles in a third column extending from the first side of the integrated circuit die to the second side of the integrated circuit die, the plurality of tiles in the third column having different functions than the function of the first column</u>.

22. (Previously Presented) The method of Claim 21, further comprising:

providing a first input/output block on a first side of the first column; and

providing a second input/output block on a second side of the first column.

23. (Previously Presented) The method of Claim 21, wherein there is no input/output block disposed between the column of configurable logic blocks and the first side of the integrated circuit die.

24. (Previously Presented) The method of Claim 21, wherein the first column includes the plurality of configurable logic blocks as well as a plurality of clock distribution tiles.

25. (Previously Presented) The method of Claim 21, wherein over ninety-five percent of the die area of the first column is occupied by configurable logic blocks.

26. (Currently Amended) An integrated circuit, comprising:

a first column of input/output block tiles, wherein the first column of input/output tiles occupies a die area, and wherein over ninety-five percent of the die area of the column is occupied by input/output block tiles;

a first configurable logic block tile disposed on a first side of the first column; [[and]]

a second configurable logic block tile disposed on a second side of the first column opposite the first side; and

a second column of input/output block tiles disposed on an end of the integrated circuit.

27. (Currently Amended) The integrated circuit of Claim 26, wherein each of the input/output block tiles in the first column has an identical layout.

28. (Original) The integrated circuit of Claim 26, wherein the integrated circuit is a field programmable gate array.

29. (Previously Presented) The integrated circuit of Claim 26, wherein the integrated circuit is disposed on a semiconductor die, the semiconductor die having a first side, a second side opposite the first side, a third side, and a fourth side opposite the third side, and wherein the first column of input/output block tiles extends from the first side and to the second side, a first input/output block tile of the first column being disposed adjacent the first side of the die, a second input/output block tile of the first column being disposed adjacent the second side of the die.

30. (Currently Amended) An integrated circuit comprising:

a plurality of configurable logic block tiles; [[and]]

a plurality of input/output block tiles disposed in columns, each of the columns extending in a first direction, wherein no two input/output block tiles of the integrated circuit are disposed adjacent to one another to form a row that extends in a second direction perpendicular to the first direction; and

a plurality of tiles disposed in a column on an end of the integrated circuit, wherein the plurality of tiles comprises a plurality of transceivers.

31. (Original) The integrated circuit of Claim 30, wherein the integrated circuit comprises at least three columns of input/output block tiles.

32. (Currently Amended) An integrated circuit consisting essentially of tiles, the integrated circuit comprising:

an input/output block tile having four sides and in a column of input/output block tiles extending from a first end to a second end, wherein the input/output block tile is bounded on each of its four sides by another tile; and

a plurality of tiles in a second column extending from a first end to a second end, wherein the plurality of tiles comprises memory cells.

Claims 33-34. (Cancelled)